What is claimed is:

1. A nonvolatile memory microcomputer chip comprising a microcomputer unit and a memory unit,

the microcomputer unit including:

a plurality of circuit blocks including a CPU, and

the memory unit including:

a nonvolatile memory;

a memory control unit operable to (a) acquire a plurality of pieces of test data from outside the nonvolatile memory microcomputer chip and store the plurality of pieces of test data in the nonvolatile memory, and then (b) control the nonvolatile memory to sequentially output a plurality of test signals which each show a piece of test data out of the plurality of pieces of test data;

a drive unit operable to supply each of the plurality of test signals sequentially output from the nonvolatile memory, to any of the plurality of circuit blocks that is to be tested using a piece of test data shown by the test signal, to drive the circuit block; and

an output unit operable to receive a test result signal from the driven circuit block, and output the test result signal to outside the nonvolatile memory microcomputer chip.

2. The nonvolatile memory microcomputer chip of Claim 1,

wherein the microcomputer unit further includes:

a port operable to send/receive a signal to/from outside the microcomputer unit,

the drive unit supplies the test signal to the circuit block through the port, and

the output unit receives the test result signal from the circuit block through the port.

3. The nonvolatile memory microcomputer chip of Claim 2,

wherein the memory control unit (a) acquires a plurality of pieces of expectation data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of expectation data in a memory area of the nonvolatile memory having a unique address, each piece of expectation data representing a test result signal that is expected if a circuit block to which a test signal showing a corresponding piece of test data is output is driven correctly, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and an expectation signal that respectively show a piece of test data and a piece of expectation data stored in a memory area having an address shown by the address

signal,

the drive unit supplies the test signal output from the nonvolatile memory in response to the address signal, to a circuit block that is to be tested using the piece of test data shown by the test signal, to drive the circuit block, and

the output unit receives a test result signal from the driven circuit block, and outputs the test result signal and the expectation signal together to outside the nonvolatile memory microcomputer chip.

4. The nonvolatile memory microcomputer chip of Claim 1, further comprising:

an address generation unit operable to sequentially output a plurality of address signals,

the memory control unit (a) stores each piece of test data in a memory area of the nonvolatile memory having a unique address, and then (b) each time the address generation unit outputs an address signal, controls the nonvolatile memory to output a test signal showing a piece of test data stored in a memory area having an address shown by the address signal, and

the drive unit supplies the test signal output from the nonvolatile memory in response to the address signal, to a circuit block that is to be tested using the piece

of test data shown by the test signal, to drive the circuit block.

5. The nonvolatile memory microcomputer chip of Claim 4,

wherein the memory control unit (a) acquires a plurality of pieces of control data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of control data in a memory area of the nonvolatile memory in which a corresponding piece of test data is stored, the plurality of pieces of control data designating an order in which the plurality of pieces of test data are used, and then (b) each time the address generation unit outputs an address signal, controls the nonvolatile memory to output a test signal and a control signal which respectively show a piece of test data and a piece of control data stored in a memory area having an address shown by the address signal, and

the address generation unit includes:

a counter unit holding a count value, and operable to periodically output an address signal showing the count value and increment the count value by 1; and

a counter control unit operable to (i) store the count value held by the counter unit when the nonvolatile memory outputs a control signal showing a piece of control data

having a first value, and subsequently (ii) replaces the count value held by the counter unit with the stored count value when the nonvolatile memory outputs a control signal showing a piece of control data having a second value.

6. The nonvolatile memory microcomputer chip of Claim 4,

wherein the plurality of pieces of test data are divided into test data groups, with a piece of test data at the end of each test data group being end data that can be distinguished from other pieces of test data, and

the address generation unit includes:

an address storage unit operable to store an address of a memory area of the nonvolatile memory in which a piece of test data at the beginning of each test data group is stored;

a counter unit holding a count value, and operable to periodically output an address signal showing the count value and increment the count value by 1; and

a counter control unit operable to replace the count value held by the counter unit with one of addresses stored in the address storage unit, when the nonvolatile memory outputs a test signal showing the end data.

7. The nonvolatile memory microcomputer chip of Claim 4,

wherein the plurality of pieces of test data are

divided into test data groups, with a piece of test data at the end of each test data group being end data that can be distinguished from other pieces of test data,

the address generation unit includes:

an address storage unit operable to acquire a plurality of addresses and a plurality of control flag values which are in a one-to-one correspondence with each other from outside the nonvolatile memory microcomputer chip, and store the plurality of addresses and the plurality of control flag values beforehand; and

a release signal acquisition unit operable to acquire a release signal from outside the nonvolatile memory microcomputer chip, and

the address generation unit, for each address stored in the address storage unit,

(1) outputs an address signal showing the address,

(2) if a corresponding control flag value is a first value, subsequently outputs address signals which show consecutive addresses following the address in sequence, until the nonvolatile memory outputs a test signal showing the end data, and

(3) if the corresponding control flag value is a second value, subsequently outputs address signals which uniformly show the address in sequence, until the release signal acquisition unit acquires the release signal.

8. The nonvolatile memory microcomputer chip of Claim 1, wherein the memory control unit includes:

an address adjustment unit operable to:

(1) hold a repetition start address, a repetition end address, and a repetition number;

(2) sequentially receive a plurality of address signals; and

(3) each time an address signal is received, (i) output the address signal if an address shown by the address signal is different from the repetition start address, and (ii) repeat, a number of times equivalent to the repetition number, outputting address signals which show consecutive addresses from the repetition start address to the repetition end address in sequence, if the address shown by the address signal is same as the repetition start address,

the memory control unit (a) stores each piece of test data in a memory area of the nonvolatile memory having a unique address, and then (b) each time the address adjustment unit outputs an address signal, controls the nonvolatile memory to output a test signal showing a piece of test data stored in a memory area having an address shown by the address signal, and

the drive unit supplies the test signal output from

the nonvolatile memory in response to the address signal, to a circuit block that is to be tested using the piece of test data shown by the test signal, to drive the circuit block.

9. The nonvolatile memory microcomputer chip of Claim 3,

wherein at least two pieces of test data out of the plurality of pieces of test data have different bit lengths according to different contents of the at least two pieces of test data,

the drive unit supplies a mixed signal to the port, the mixed signal being made up of a test signal showing a piece of test data whose bit length is not largest among the plurality of pieces of test data and one part of an expectation signal output from the nonvolatile memory together with the test signal, and

the port extracts the test signal from the mixed signal according to contents of the mixed signal, and supplies the extracted test signal to a circuit block that is to be tested using the piece of test data shown by the test signal.

10. The nonvolatile memory microcomputer chip of Claim 1,

wherein the drive unit shifts the test signal in level

based on an input signal reference voltage applied from outside the nonvolatile memory microcomputer chip, and supplies the shifted test signal to the circuit block to drive the circuit block, and

the output unit shifts the test result signal in level based on a comparison reference voltage applied from outside the nonvolatile memory microcomputer chip, and outputs the shifted test result signal to outside the nonvolatile memory microcomputer chip.

11. The nonvolatile memory microcomputer chip of Claim 1, further comprising:

a plurality of pairs of connection lines which are provided in a one-to-one correspondence with the plurality of circuit blocks, and each operable to transfer a signal between a corresponding circuit block and the drive unit and between the corresponding circuit block and the output unit,

the drive unit supplies the test signal to the circuit block through one connection line out of a pair of connection lines corresponding to the circuit block, and

the output unit receives the test result signal from the circuit block through the other connection line out of the pair of connection lines corresponding to the circuit block.

12. The nonvolatile memory microcomputer chip of Claim 11,

wherein the memory control unit (a) stores each piece of test data in a memory area of the nonvolatile memory having a unique address, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal showing a piece of test data stored in a memory area having an address shown by the address signal,

the memory unit further includes:

a circuit block specification unit operable to specify a circuit block that is to be tested using the piece of test data shown by the test signal output from the nonvolatile memory in response to the address signal, based on the address signal, and

the drive unit supplies the test signal to the circuit block specified by the circuit block specification unit, to drive the circuit block.

13. The nonvolatile memory microcomputer chip of Claim 11,

wherein the memory control unit (a) acquires a plurality of pieces of selection data from outside the

nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory having a unique address, each piece of selection data being used for specifying a circuit block that is to be tested using a corresponding piece of test data, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and a selection signal which respectively show a piece of test data and a piece of selection data stored in a memory area having an address shown by the address signal, and

the drive unit supplies the test signal output from the nonvolatile memory in response to the address signal, to a circuit block that is specified according to the selection signal, to drive the circuit block.

14. The nonvolatile memory microcomputer chip of Claim 1,

wherein the memory unit includes a plurality of nonvolatile memories,

the memory control unit (a) stores the plurality of pieces of test data in the plurality of nonvolatile memories,

and then (b) controls each nonvolatile memory to sequentially output a plurality of test signals which each show a piece of test data out of pieces of test data stored in the nonvolatile memory, in parallel,

wherein if two nonvolatile memories out of the plurality of nonvolatile memories are to output test signals showing pieces of test data used for testing a same circuit block, the memory control unit allows one of the two nonvolatile memories to output a test signal and prohibits the other nonvolatile memory from outputting a test signal, and

the drive unit supplies a test signal output from each nonvolatile memory, to a circuit block that is to be tested using a piece of test data shown by the test signal, to drive the circuit block.

15. The nonvolatile memory microcomputer chip of Claim 1,

wherein the nonvolatile memory includes:

an oscillation circuit operable to generate a first clock signal, and

the nonvolatile memory microcomputer chip further comprises:

a selection circuit operable to selectively supply one of the first clock signal and a second clock signal

which is fed from outside the nonvolatile memory microcomputer chip, to each circuit block in the microcomputer unit.

16. The nonvolatile memory microcomputer chip of Claim 15,

wherein the memory control unit (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory having a unique address, each piece of selection data being used for selecting one of the first clock signal and the second clock signal, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and a selection signal which respectively show a piece of test data and a piece of selection data stored in a memory area having an address shown by the address signal, and

the selection circuit supplies one of the first clock signal and the second clock signal that is selected according to the selection signal, to each circuit block in the microcomputer unit.

17. The nonvolatile memory microcomputer chip of Claim 15,

wherein the memory control unit (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory having a unique address, each piece of selection data being used for selecting a frequency of the first clock signal, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and a selection signal which respectively show a piece of test data and a piece of selection data stored in a memory area having an address shown by the address signal, and

the oscillation circuit generates the first clock signal having a frequency that is selected from a plurality of predetermined frequencies according to the selection signal.

18. The nonvolatile memory microcomputer chip of Claim 1,

wherein the memory control unit (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory having a unique address, each piece of selection data being used for selecting a delay time, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and a selection signal which respectively show a piece of test data and a piece of selection data stored in a memory area having an address shown by the address signal,

the output unit includes:

a delay unit operable to delay a test result signal received from a circuit block which is driven by the test signal output from the nonvolatile memory in response to the address signal, by a delay time that is selected from a plurality of predetermined delay times according to the selection signal, and

the output unit outputs the delayed test result signal to outside the nonvolatile memory microcomputer chip.

19. The nonvolatile memory microcomputer chip of Claim

1,

wherein the memory control unit (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory having a unique address, each piece of selection data being used for selecting a delay time, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and a selection signal which respectively show a piece of test data and a piece of selection data stored in a memory area having an address shown by the address signal,

the drive unit includes:

a delay unit operable to delay the test signal output from the nonvolatile memory in response to the address signal, by a delay time that is selected from a plurality of predetermined delay times according to the selection signal, and

the drive unit supplies the delayed test signal to a circuit block that is to be tested using the piece of test data shown by the delayed test signal, to drive the circuit block.

20. The nonvolatile memory microcomputer chip of Claim 1,

wherein the memory control unit (a) acquires a plurality of pieces of designation data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of designation data in a memory area of the nonvolatile memory having a unique address, each piece of designation data being used for designating a voltage, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and a designation signal which respectively show a piece of test data and a piece of designation data stored in a memory area having an address shown by the address signal, and

the nonvolatile memory microcomputer chip further comprises:

a power supply unit operable to adjust a voltage of external power applied from outside the nonvolatile memory microcomputer chip to a voltage that is designated according to the designation signal to generate internal power, and supply the internal power to a circuit block

that is to be tested using the piece of test data shown by the test signal as operating power.

21. The nonvolatile memory microcomputer chip of Claim 20,

wherein the plurality of circuit blocks in the microcomputer unit include:

a D/A conversion circuit which serves as the power supply unit,

wherein the D/A conversion circuit generates the internal power by digital-to-analog converting the piece of designation data shown by the designation signal, and supplies the internal power to the circuit block as the operating power.

22. The nonvolatile memory microcomputer chip of Claim 20,

wherein the nonvolatile memory includes a power circuit which serves as the power supply unit,

wherein the power circuit includes:

a step-up circuit operable to step-up the voltage of the external power; and

a voltage adjustment circuit operable to generate the internal power by stepping-down the stepped-up voltage of the external power to the voltage designated according

to the designation signal, and supply the internal power to the circuit block as the operating power.

23. The nonvolatile memory microcomputer chip of Claim 1,

wherein the memory control unit (a) acquires a plurality of pieces of designation data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of designation data in a memory area of the nonvolatile memory having a unique address, each piece of designation data being used for designating a current, and then (b) each time an address signal is given from outside the nonvolatile memory microcomputer chip, controls the nonvolatile memory to output a test signal and a designation signal which respectively show a piece of test data and a piece of designation data stored in a memory area having an address shown by the address signal,

the nonvolatile memory microcomputer chip further comprises:

a current judgment unit operable to judge whether a power supply current applied to the microcomputer unit exceeds a current designated according to the designation signal, and output a current judgment signal showing a

result of the judgment, and

the output unit receives the current judgment signal from the current judgment unit, and outputs the current judgment signal to outside the nonvolatile memory microcomputer chip together with a test result signal received from a circuit block which is driven by the test signal.

24. The nonvolatile memory microcomputer chip of Claim 23,

wherein the nonvolatile memory includes:

a sense amplifier through which the power supply current passes, and which serves as the current judgment unit,

wherein the sense amplifier generates a reference current according to the designation signal, and outputs the current judgment signal based on a comparison between the reference current and the power supply current.

25. The nonvolatile memory microcomputer chip of Claim 3,

wherein when a defective signal is given from outside the nonvolatile memory microcomputer chip in response to the test result signal and the expectation signal, the memory control unit stores the address shown by the address

signal to a predetermined memory area of the nonvolatile memory, the defective signal indicating that the circuit block is judged as being defective as a result of testing.

26. The nonvolatile memory microcomputer chip of Claim 25,

wherein the memory control unit (a) acquires a plurality of instructions which constitute a program that is executable by the CPU, from outside the nonvolatile memory microcomputer chip, and stores each instruction in a memory area of the nonvolatile memory having a unique address, and then (b) when the defective signal is given from outside the nonvolatile memory microcomputer chip, stores the address shown by the address signal to the predetermined memory area of the nonvolatile memory, and subsequently supplies a control signal to the CPU, the control signal instructing to execute the program from an address of a memory area storing a beginning instruction.

27. The nonvolatile memory microcomputer chip of Claim 4,

wherein the memory control unit supplies a data signal showing a non-operation instruction, to the CPU, and

the CPU executes the non-operation instruction shown by the data signal a plurality of times to sequentially

output address signals which show consecutive addresses, thereby serving as the address generation unit.

28. A method for testing a nonvolatile memory microcomputer chip including a microcomputer unit and a nonvolatile memory unit, comprising:

a first test step of storing first test data in the nonvolatile memory unit, and then testing the microcomputer unit using the first test data in the nonvolatile memory unit to judge whether the microcomputer unit is defective; and

a second test step of storing, if the microcomputer unit is judged as being defective in the first test step, replacing the first test data in the nonvolatile memory unit with second test data, and then testing the microcomputer unit using the second test data in the nonvolatile memory unit.

29. A method for testing a plurality of nonvolatile memory microcomputer chips which each include a microcomputer unit and a nonvolatile memory unit, comprising:

a first test step of selecting a part of the plurality of nonvolatile memory microcomputer chips as test samples, storing first test data for performing testing about at least one test item in a nonvolatile memory unit of each

test sample, and then testing a microcomputer unit of each test sample using the first test data stored in the nonvolatile memory unit for each test item;

a decision step of deciding, for each test item, whether all of the plurality of nonvolatile memory microcomputer chips need to be tested, based on a result of the testing in the first test step; and

a second test step of storing second test data for performing testing about each test item for which all of the plurality of nonvolatile memory microcomputer chips are decided as needing to be tested, to a nonvolatile memory unit of each of the plurality of nonvolatile memory microcomputer chips, and then testing a microcomputer unit of each of the plurality of nonvolatile memory microcomputer chips using the second test data stored in the nonvolatile memory unit.

30. A method for testing a first nonvolatile memory microcomputer chip and a second nonvolatile memory microcomputer chip which each include a microcomputer unit and a nonvolatile memory unit, where the first and second nonvolatile memory microcomputer chips are connected so that data stored in a nonvolatile memory unit of the second nonvolatile memory microcomputer chip can be supplied to a microcomputer unit of the first nonvolatile memory

microcomputer chip, comprising:

a storage step of storing first test data for performing testing about a first test item in a nonvolatile memory unit of the first nonvolatile memory microcomputer chip, and storing second test data for performing testing about a second test item in the nonvolatile memory unit of the second nonvolatile memory microcomputer chip;

a first test step of testing the microcomputer unit of the first nonvolatile memory microcomputer chip using the first test data stored in the nonvolatile memory unit of the first nonvolatile memory microcomputer chip;

a supply step of supplying the second test data stored in the nonvolatile memory unit of the second nonvolatile memory microcomputer chip, to the microcomputer unit of the first nonvolatile memory microcomputer chip; and

a second test step of testing the microcomputer unit of the first nonvolatile memory microcomputer chip using the second test data supplied from the nonvolatile memory unit of the second nonvolatile memory microcomputer chip.